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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/747,957	12/27/2000	Tadayoshi Kono	108391-00014	3190

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EXAMINER	
VO, TUNG T	

ART UNIT	PAPER NUMBER
2613	

DATE MAILED: 01/09/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/747,957	KONO ET AL.	
	Examiner	Art Unit	
	Tung Vo	2613	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 December 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3 and 5-12* is/are pending in the application.

4a) Of the above claim(s) *4* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3 and 5-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 12/05/05 has been entered.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. '103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-3 and 5-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takabatake et al. (US 6,320,909) in view of Mendenhall et al. (US 6,424,381 B1).

Re claims 1, 3, 5, and 9-10, Takabatake discloses an MPEG video decoder for an MPEG bit stream into which a picture is encoded, the MPEG video decoder (fig. 1) comprising:

an image decoding section (10 of fig. 1) which decodes the MPEG bit stream to obtain the picture and parameters of each laver, wherein the parameters include parameters of a sequence laver, the parameters of the sequence laver includes a horizontal size value and a vertical size value of the picture, and

a frame memory (12 of fig. 1) having a plurality of banks (32, 34, and 36 of fig. 1) and connected to the image decoding section, wherein each of said the banks has an area (BANK # 1 of fig. 1) for storing the picture and the parameters obtained by said the image decoding section, and stores the picture and the parameters by mutually relating the picture and the parameters as a set (storing I, P, B; col. 10, lines 48-55);

a decode control section (14 of fig. 1) which controls said the image decoding section;

a display control section (20 of fig. 1) connected to the decode control section and to the frame memory, wherein the display control section carries out a display control the picture stored in the frame memory based on the parameters (picture header) stored in said the frame memory; and

a status register (16 of figs. 1 and 9) for storing values indicating whether display of the picture stored in the frame memory has finished, wherein the status register has an arbitration function (14 of fig. 1, wherein the control unit (14) has an arbitration function of adjusting address generation timings of the address generators (50, 52 and 54 of fig. 9) for preventing the addresses thereof from confliction on the address bus. Alternatively, an arbiter for avoiding access confliction on the memory device 12 may be separately provided)for arbitrating between the decode control section and the display control section (the selector which is included in the delay switching circuit (80 of fig. 23) simply implement the function of passing the signal, and hence it may have an arbitrary circuit structure. Namely, the selector may only have a structure of effectuating the delay provided by the delay circuit (60 of fig. 23) for decoding and displaying frame structure pictures, while invalidating the delay for decoding and displaying field structure

pictures), and overwriting the first parameters with the second parameters (fig. 17; Note overwriting of the pixel data is prevented in bank #3 (see FIG. 1) for storing B frames).

It is noted that the decoding section (10 of fig. 1) for transferring the decoded picture and parameters (picture and macroblocks headers) to the memory (12 of fig.1) as a data transfer path for transferring the picture from the image decoding section to said the frame memory also works as a data transfer path for transferring the parameters of each layer between said the image decoding section and said frame memory.

However, Takabatake does not particularly disclose the image decoding section includes an internal buffer for temporarily storing the picture, the parameters and macroblocks as claimed.

Mendenhall teaches wherein said internal buffer also works as a buffer for temporarily storing the decoded parameters of each layer (col. 7, lines 20-30; Note the decoder (130 of fig. 6) includes buffers for storing the decoded image and each of the syntax layers).

Therefore, taking the teachings of Takabatake and Mendenhall as a whole, it would have been obvious to one of ordinary skill in the art to incorporate the decoding buffer of Mendenhall into the image decoding section of Takabatake for temporally storing the decoded images and transferring to the memory. Doing so would control the decoding efficiency.

Re claim 2, Takabatake further teaches wherein the status register indicates a data storage state of each bank (32, 34, and 36 of fig. 1, storing I, P, and B), and the decode control section (14 of fig. 1) updates said the status register when the picture is obtained, and said the display control section (20 of fig. 1) updates said the status register when the picture is displayed (Note In a period T1, the decoding/display circuit DDC is supplied with picture data of an I picture I3, to decode the data. The decoded picture data of the I picture I3 are written in the bank #1 (BA1)

of the memory device MR. Upon completion of the period T1, the bank #1 stores all pixel data of the I picture I3).

Re claim 6, Takabatake further teaches wherein decoding section decodes the MPEG bit stream to obtain first parameters and overwrites second parameters obtained immediately before with the first parameters (fig. 17; Note Overwriting of the pixel data is prevented in bank #3 (see FIG. 1) for storing B frames).

Re claim 7 Takabatake further teaches wherein said the decode control section operates asynchronously with a vertical synchronization signal, and said the display control section operates in synchronism with the vertical synchronization signal (HSYNC and VSYNC of fig. 1).

Re claim 8, Takabatake further teaches wherein control section does not update said the status register wherein a reference picture of other pictures is displayed (while the reference pictures is displayed, the control section does not perform of updating).

Re claims 11 and 12, Takabatake further teaches MPEG stream that includes at least one layer of a GOP layer, sequence layer, and picture layer (fig. 29).

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Mendenhall et al. (US 6,570,626) discloses on-screen display format reduces memory bandwidth for on-screen display systems.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tung Vo whose telephone number is 571-272-7340. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mehrdad Dastouri can be reached on 571-272-7418. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tung Vo
Primary Examiner
Art Unit 2613